CLAIMS

1. A digital arithmetic operation circuit comprising:

a plurality of arithmetic operation blocks for receiving a plurality of digital input signals and for performing different arithmetic operations on said received digital input signals, in parallel, to output operation result signals;

a control signal generator for receiving a plurality of digital input signals and for generating a control signal based on said digital input signals; and

a selector, connected to said plurality of arithmetic operation blocks and said control signal generator, for selecting one of said operation result signals, in response to said control signal, to output said selected operation result signal,

wherein after said control signal generator supplies said control signal to said selector, said selector outputs said selected operation result signal as soon as said selected operation result signal is supplied to said selector.

2. A maximum likelihood decoder comprising:

a plurality of arithmetic operation blocks for receiving a plurality of digital input signals and for performing maximum likelihood decoding operations on said received digital input signals, in parallel according to a carry save system, to output decoded signals;

a control signal generator for receiving a plurality of digital input signals and for performing an arithmetic operation on said received digital input signals according to a carry look ahead system, to generate a control signal indicative of a most significant bit of an operation result; and

a selector, connected to said plurality of arithmetic operation blocks and said control signal generator, for selecting one of said decoded signals in response to said control signal, to output said selected decoded signal.

3. A semiconductor integrated circuit comprising:

an analog equalizer filter for receiving an analog signal and for adjusting a level of said analog signal to output an equalized filtered analog signal;

an A/D converter, connected to said analog equalizer filter, for converting said equalized filtered analog signal to a digital signal;

a digital filter, connected to said A/D converter, for receiving said digital signal and for removing an unnecessary digital components from said digital signal to output a filtered digital signal;

a maximum likelihood decoder, connected to said digital filter, for receiving said filtered digital signal and for performing a maximum likelihood decoding operation on said received filtered digital signal to generate a serial decoded signal;

a serial-parallel converter, connected to said maximum likelihood decoder, for converting said serial decoded signal to a parallel decoded signal; and

a channel characteristic generator, operatively connected to said maximum likelihood decoder in a test mode, for receiving a test signal supplied from an external testing device and for generating a test version of said filtered digital signal from said test signal, wherein in said test mode, said maximum likelihood decoder receives said test filtered digital signal and performs maximum likelihood decoding thereon.

4. The semiconductor integrated circuit according to Claim 3, wherein said external testing device outputs a first clock signal,

wherein said semiconductor integrated circuit further comprises a clock generator, connected to said maximum likelihood decoder, said serial-parallel converter and said channel characteristic generator, for generating a second clock signal having a higher frequency than said first clock signal,

wherein said maximum likelihood decoder, said serial-parallel converter and said channel characteristic generator operate in response to said second clock signal.

5. The semiconductor integrated circuit according to Claim 3, wherein said analog signal is read from a recording medium, said test signal is a parallel signal equivalent to a write signal to be written on said recording medium, and said channel characteristic generator includes:

a parallel-serial converter for converting said parallel test signal to a serial signal;

a first characteristic generation circuit, connected to said parallel-serial converter, for generating a first signal having a channel characteristic of a write circuit for said recording medium, from said serial signal;

a second characteristic generation circuit, connected to said first characteristic generation circuit, for generating a second signal having a channel characteristic of a read circuit for said recording medium, from said first signal;

a third characteristic generation circuit, connected to said second characteristic generation circuit, for generating a third signal having a channel characteristic of said analog equalizer filter from said second signal; and

a fourth characteristic generation circuit, connected to said third characteristic generation circuit, for generating a test filtered digital signal having a channel characteristic of said digital filter from said third signal.

6. The semiconductor integrated circuit according to Claim 3, wherein said maximum likelihood decoder includes:

a plurality of arithmetic operation blocks for receiving a plurality of digital input signals including said filtered digital signal and for performing maximum likelihood decoding operations on said received digital input signals according to a carry save system in parallel to output serial decoded signals;

a control signal generation circuit for receiving a plurality of digital input signals and for performing an arithmetic operation on said received digital input signals according to a carry look ahead system, to generate a control signal indicative of a most significant bit of an operation result; and

a selector, connected to said plurality of arithmetic operation blocks and said control signal generation circuit, for selecting one of said serial decoded signals in response to said control signal, to output said selected serial decoded signal to said serial-parallel converter.

7. A semiconductor integrated circuit device comprising:

an input data holding circuit for temporarily holding an input data signal and for outputting said held input data signal in accordance with a system clock signal;

an internal circuit block, connected to said input data holding circuit, for receiving said input data signal and for performing a predetermined data processing operation to output

an output data signal in accordance with said system clock signal;

an output data holding circuit, connected to said internal circuit block, for temporarily holding said output data signal and for outputting said held output data signal in accordance with said system clock signal, wherein said input data holding circuit and said output data holding circuit are operable in accordance with a scan clock signal having a frequency lower than said system clock signal; and

an external interface circuit connected to said internal circuit block, said input data holding circuit and said output data holding circuit and responsive to said scan clock signal, for generating a test clock signal having a frequency higher than that of said scan clock signal and equal to or higher than that of said system clock signal,

wherein said external interface circuit supplies said scan clock signal and a test data signal to said input data holding circuit in such a way that said test data signal, as said input data signal, is temporarily held and is output in accordance with said scan clock signal, supplies said test clock signal to said internal circuit block in such a way that said test data signal is processed in accordance with said test clock signal, and supplies said scan clock signal to said output data holding circuit in such a way that a test result signal, as an output data signal, is temporarily held and is output in accordance with said scan clock signal.

8. The semiconductor integrated circuit device according to Claim 7, wherein said input data holding circuit includes a selector for receiving a normal data signal and a test data signal, both included in said input data signal, and for selecting one of said normal data signal and test data signal.

9. The semiconductor integrated circuit device according to Claim 7, wherein each of said input data holding circuit and said output data holding circuit includes a first-in-first-out (FIFO) register.

10. A semiconductor integrated circuit device comprising:

an internal circuit block for receiving an analog input data signal and for performing a processing operation on said analog input data signal to output a digital output data signal in accordance with a system clock signal;

an output data holding circuit, connected to said internal circuit block, for temporarily holding said digital output data signal and for outputting said held digital output data signal in accordance with said system clock signal, wherein said output data holding circuit is operable in accordance with a scan clock signal having a frequency lower than said system clock signal; and

an external interface circuit connected to said internal circuit block and said output data holding circuit and responsive to said scan clock signal, for generating a test clock signal having a frequency higher than that of said scan clock signal and equal to or higher than that of said system clock signal,

wherein said external interface circuit supplies said test clock signal to said internal circuit block in such a way that a test data signal, as said analog input data signal, is processed in accordance with said test clock signal, and supplies said scan clock signal to said output data holding circuit in such a way that a test result signal as said digital output data signal is temporarily held and is output in accordance with said scan clock signal.

11. The semiconductor integrated circuit device according to Claim 10, wherein said output data holding circuit includes a first-in-first-out (FIFO) register.

12. A semiconductor integrated circuit device comprising:

an input data holding circuit for temporarily holding a digital input data signal and for outputting said held digital input data signal in accordance with a system clock signal, said input data holding circuit being operable in accordance with a scan clock signal having a frequency lower than said system clock signal;

an internal circuit block for receiving said digital input data signal and for performing a predetermined data processing operation on said digital input data signal to output an analog output data signal; and

an external interface circuit connected to said internal circuit block and said input data holding circuit and responsive to said scan clock signal, for generating a test clock signal having a frequency higher than that of scan clock signal and equal to or higher than that of said system clock signal,

wherein said external interface circuit supplies said scan clock signal and a test data signal to said input data holding circuit in such a way that said test data signal, as said digital input data signal, is temporarily held and is output in accordance with said scan clock signal, and supplies said test clock signal to said internal circuit block in such a way that said digital input data signal is processed in accordance with said test clock signal.

13. The semiconductor integrated circuit device according to Claim 12, further comprising a selector, connected between

said input data holding circuit and said internal circuit block, for receiving a normal data signal, as said digital input data signal, and a test data signal, as said digital input data signal, output from said input data holding circuit, and for selecting one of said normal data signal and test data signal.

14. The semiconductor integrated circuit device according to Claim 13, wherein said input data holding circuit includes a first-in-first-out (FIFO) register.

15. A semiconductor integrated circuit device comprising:

an input data holding circuit for temporarily holding a digital input data signal and for outputting said held input data signal in accordance with a system clock signal;

an internal circuit block, connected to said input data holding circuit, for receiving said digital input data signal and for processing said digital input data signal, to output an analog output data signal;

an analog-digital converter, connected to said internal circuit block, for receiving said analog output data signal and for processing said analog output data signal, to output a digital output data signal in accordance with said system clock signal;

an output data holding circuit, connected to said analog-digital converter, for temporarily holding said digital output data signal and for outputting said held digital output data signal in accordance with said system clock signal, wherein said input data holding circuit and said output data holding circuit are operable in accordance with a scan clock signal having a frequency lower than said system clock signal; and

an external interface circuit connected to said internal circuit block, said input data holding circuit and said output data holding circuit, and responsive to said scan clock signal, for generating a test clock signal having a frequency higher than that of said scan clock signal and equal to or higher than that of said system clock signal,

wherein said external interface circuit supplies said scan clock signal and a test data signal to said input data holding circuit in such a way that said test data signal, as said digital input data signal, is temporarily held and is output in accordance with said scan clock signal,
supplies said test clock signal to said internal circuit block in such a way that said test data signal is processed in accordance with said test clock signal, and supplies said scan clock signal to said output data holding circuit in such a way that a test result signal, as a digital output data signal, is temporarily held and is output in accordance with said scan clock signal.

16. The semiconductor integrated circuit device according to Claim 15, wherein both said input data holding circuit and said output data holding circuit include a first-in-first-out (FIFO) register.

17. A signal processor suitable for processing a user data signal, associated with data information read from a recording medium, and a servo data signal associated with servo information read from said recording medium, said signal processor comprising:

A) a user data signal processing circuit for processing said user data signal, said user data signal processing circuit includes,

A1) a first amplifier for amplifying said user data signal to produce an amplified user data signal, and

A2) a first filter, connected to said first amplifier, for cutting off an unnecessary frequency component included in said amplified user data signal to produce a filtered amplified user data signal; and

B) a servo data signal processing circuit for processing said servo data signal, said servo data signal processing circuit includes,

B1) a second amplifier for amplifying said servo data signal to produce an amplified servo data signal, and

B2) a second filter, connected to said second amplifier, for cutting off an unnecessary frequency component included in said amplified servo data signal to produce a filtered amplified servo data signal.

18. The signal processor according to Claim 17, wherein said user data signal has a high frequency characteristic, said first amplifier amplifies said user data signal in such a way as to emphasize the high frequency characteristic of said user data signal, said servo data signal has a low frequency characteristic, and said second amplifier amplifies said servo data signal in such a way as to emphasize the low frequency characteristic of said servo data signal.

19. The signal processor according to Claim 18, wherein said first filter cuts off a frequency component higher than the high frequency characteristic of said amplified user data signal, and said second filter cuts off a frequency component higher than said low frequency characteristic of the amplified servo data signal.

20. An integrating circuit for acquiring plural pieces of position data in order to obtain relative positions between tracks to which servo areas provided on a recording medium belong and a drive head moving over said recording medium, each servo area including a plurality of position areas where said position data are respectively recorded, said integrating circuit comprising:

a rectifier for rectifying position data signals read from said position areas to produce rectified position data signals;

a voltage-current converter, connected to said rectifier, for producing charge currents having current values proportional to voltage levels of said respective rectified position data signals;

a main capacitor, connected to said voltage-current converter, for performing charging with said charge currents;

a main charge switch connected between said voltage-current converter and said main capacitor, and operable in such a way as to permit each of said charge currents to be supplied to said main capacitor when each charge current is generated;

a main discharge switch, connected to said main capacitor, for permitting charges, stored in said main capacitor, to be discharged after said main capacitor has performed a charging operation;

a plurality of detection capacitors, connected to said voltage-current converter, for performing charging with charge voltages respectively associated with said position areas, in cooperation with said main capacitor, said charge voltages of said detection capacitors respectively indicating said plural pieces of position data;

a plurality of subcharge switches respectively connected

between said voltage-current converter and said detection capacitors and operable in such a way as to permit supply of said associated charge currents to said main capacitor when said charge currents are produced; and

a plurality of subdischarge switches, respectively connected to said plurality of subcharge switches, for permitting charges stored in said detection capacitors to be discharged after execution of charging operations of said associated detection capacitors.

21. A signal processor suitable for processing a user data signal associated with data information read from a plurality of data areas provided on a recording medium and a servo data signal associated with servo information read from a plurality of servo areas provided on said recording medium, each of said data areas and each of said servo areas forming a sector, each servo area having a plurality of position areas where plural pieces of position data included in said servo information are recorded, and a servo mark area where a servo mark included in said servo information is recorded, each position data being used to acquire a relative position between a track including a sector to which an associated servo area belongs and a drive head moving over said recording medium, said servo mark indicating a start of each sector, said servo data signal including a plurality of position data signals respectively associated with said plural pieces of position data and a servo mark signal associated with said servo mark, said signal processor comprising:

A) a user data signal processing circuit for processing said user data signal, said user data signal processing circuit including,

A1) a first amplifier for amplifying said user data

signal to produce an amplified user data signal, and

A2) a first filter, connected to said first amplifier, for cutting off an unnecessary frequency component included in said amplified user data signal to produce a filtered amplified user data signal; and

B) a servo data signal processing circuit for processing said servo data signal, said servo data signal processing circuit including,

B1) a second amplifier for amplifying said servo data signal to produce an amplified servo data signal,

B2) a second filter, connected to said second amplifier, for cutting off an unnecessary frequency component included in said amplified servo data signal to produce a filtered amplified servo data signal,

B3) a peak detector, connected to said second filter, for detecting a peak value of said servo mark signal included in said servo data signal to generate a peak signal, wherein an external device generates strobe signals indicative of read timings of said individual position data in accordance with said peak signal,

B4) a zero-cross detector, connected to said second filter, for receiving each position data signal included in said servo data signal and producing a clock signal,

B5) a rectifier, connected to said second filter, for rectifying said position data signals to produce rectified position data signals;

B6) a voltage-current converter, connected to said rectifier, for producing charge currents having current values proportional to voltage levels of said respective rectified position data signals;

B7) a main capacitor, connected to said voltage-current converter, for performing charging with said charge

currents;

B8) a main charge switch connected between said voltage-current converter and said main capacitor,

B9) a main discharge switch connected to said main capacitor,

B10) a plurality of detection capacitors, connected to said voltage-current converter, for performing charging with charge currents respectively associated with said position areas, in cooperation with said main capacitor, charge voltages of said detection capacitors being equivalent to integral values respectively indicating said plural pieces of position data;

B11) a plurality of subcharge switches respectively connected between said voltage-current converter and said detection capacitors,

B12) a plurality of subdischarge switches, respectively connected to said detection capacitors, and

B13) a control circuit, connected to said main charge switch, said main discharge switch, said subcharge switches and said subdischarge switches, and responsive to said strobe signals and said clock signal, wherein said control circuit controls said main charge switch in response to said strobe signals in such a way as to permit supply of said charge currents to said main capacitor, controls said main discharge switch in such a way as to permit discharging of charges stored in said main capacitor after charging of said main capacitor has been performed, controls said subcharge switches in response to said strobe signals and said clock signal in such a way as to permit supply of said associated charge currents to said detection capacitors respectively, and controls said subdischarge switches in such a way as to permit discharging of charges stored in said

detection capacitors after execution of charging of said detection capacitors.

22. The signal processor according to Claim 21, wherein said detection capacitors are connected in parallel to said main capacitor and have capacitances smaller than that of said main capacitor.

23. The signal processor according to Claim 21, wherein said control circuit switches on said subcharge switches upon each reception of said strobe signals, in such a way as to permit supply of said associated charge currents to said detection capacitors within a half period of said clock signal, counts a charge time of each of said detection capacitor in accordance with said clock signal, and switches off an associated one of said subcharge switches when a count value reaches a predetermined value.

24. The signal processor according to Claim 23, wherein when said count value does not reach said predetermined value due to a failure of generation of a clock signal by said zero-cross detector, said control circuit outputs an abnormal signal and switches off an associated one of said subcharge switches.

25. A circuit suitable for canceling an offset voltage of an A/D converter that converts an analog signal to a digital signal, said circuit comprising:

a comparator for receiving said digital signal and for comparing a digital value of said digital signal with a predetermined offset allowance value to output a comparison result;

an arithmetic operation unit, connected to said comparator, for accumulating a predetermined offset change amount and outputting an addition result based on said comparison result when said digital value differs from said predetermined offset allowance values, wherein said addition result is initially determined by adding said predetermined offset change amount and a predetermined initial value; and

an offset voltage generator, connected to said arithmetic operation unit, for generating an offset cancel voltage in order to cancel said offset voltage in accordance with said addition result and for supplying said offset cancel voltage to said A/D converter.

26. A signal processor for receiving data information as an analog signal and processing said analog signal, comprising:

an A/D converter for converting said analog signal to a digital signal;

an offset cancel circuit, connected to said A/D converter, for supplying a voltage to cancel an offset voltage of said A/D converter, said offset cancel circuit including,

a comparator for receiving said digital signal, and for comparing a digital value of said digital signal with a predetermined offset allowance value to output a comparison result;

an arithmetic operation unit, connected to said comparator, for accumulating a predetermined offset change amount and for outputting an addition result based on said comparison result, when said digital value differs from said predetermined offset allowance value, said addition result being initially determined by adding said predetermined offset change amount and a predetermined initial value; and

an offset voltage generator, connected to said

arithmetic operation unit, for generating an offset cancel voltage in order to cancel said offset voltage in accordance with said addition result and for supplying said offset cancel voltage to said A/D converter.

27. A signal processor for processing a data information signal and a servo information signal, both read from a recording medium, said signal processor comprising:

a servo information processing circuit for processing servo information; and

a data information processing circuit, connected to said servo information processing circuit, for receiving data information as an analog signal and for processing said analog signal, said data information processing circuit includes,

A) an A/D converter for receiving said analog signal from an input terminal and for converting said analog signal to a digital signal, to output said digital signal from an output terminal;

B) a switch connected to said input terminal of said A/D converter; and

C) an offset cancel circuit, connected between said input terminal and an output terminal of said A/D converter, for supplying a voltage to cancel an offset voltage of said A/D converter, said offset cancel circuit includes,

C1) a control circuit, connected to said switch, for setting said switch off to inhibit supply of said analog signal to said A/D converter when said servo information processing circuit is performing a servo information process,

C2) a comparator connected to said comparator, for receiving said digital signal and comparing a digital value of said digital signal with a predetermined offset

allowance values, to output a comparison result,

C3) an arithmetic operation unit, connected to said comparator, for accumulating a predetermined offset change amount and outputting an addition result based on said comparison result, when said digital value differs from said predetermined offset allowance values, said addition result being initially determined by adding said predetermined offset change amount and a predetermined initial value, and

C4) an offset voltage generator connected to said arithmetic operation unit, for generating an offset cancel voltage for canceling said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter.

28. The signal processor according to Claim 27, further comprising:

D) an amplifier, connected to said input terminal of said A/D converter and said control circuit, for amplifying said analog signal and said offset cancel voltage by a first amplification factor, wherein said amplifier is capable of amplifying said offset cancel voltage by a second amplification factor which is higher than said first amplification factor,

wherein said arithmetic operation unit has a reduced offset change amount inversely proportional to an increase ratio of said first amplification factor to said second amplification factor, and wherein said control circuit is connected to said comparator and said arithmetic operation unit, and

wherein when said digital value lies within a range defined by said predetermined offset allowance value, said control circuit controls said amplifier in such a way as to

amplify said offset cancel voltage by said second amplification factor and controls said arithmetic operation unit in such a way as to perform addition based on said reduced offset change amount.

29. A circuit suitable for canceling an offset voltage of an A/D converter, said A/D converter samples an analog data signal including an analog sinusoidal signal in order to convert said analog data signal to a digital signal, said circuit comprising:

a sampling control circuit for controlling said A/D converter in such a manner that first and third sampling intervals and second and fourth sampling intervals for said analog sinusoidal signal become 180 degrees when said analog sinusoidal signal is supplied to said A/D converter, whereby digital signals having first through fourth digital values are output from said A/D converter in a sampling order;

an arithmetic operation unit for receiving one of a set of said first and third digital values and a set of said second and fourth digital values, and for computing an average value thereof to output said obtained average value as an offset voltage value for said A/D converter; and

an offset voltage generator for receiving said offset voltage value, for generating an offset cancel voltage to cancel said offset voltage, and for supplying said offset cancel voltage to said A/D converter.

30. A signal processor for receiving an analog data signal including an analog sinusoidal signal recorded on a recording medium, and processing said analog data signal, said signal processor comprising:

an A/D converter for converting said analog sinusoidal

signal and said analog data signal to digital signals; and

an offset cancel circuit, connected to said A/D converter, for supplying a voltage to cancel an offset voltage of said A/D converter, said offset cancel circuit includes,

a sampling control circuit for controlling said A/D converter in such a manner that first and third sampling intervals and second and fourth sampling intervals for said analog sinusoidal signal become 180 degrees when said analog sinusoidal signal is supplied to said A/D converter, whereby digital signals having first through fourth digital values are output from said A/D converter in a sampling order;

an arithmetic operation unit for receiving one of a set of said first and third digital values and a set of said second and fourth digital values, and for computing an average value thereof to output said obtained average value as an offset voltage value for said A/D converter; and

an offset voltage generator for receiving said offset voltage value, for generating an offset cancel voltage to cancel said offset voltage, and for supplying said offset cancel voltage to said A/D converter.

31. A signal processor for processing a data information signal and a servo information signal, both read from a recording medium, said signal processor comprising:

a servo information processing circuit for processing servo information,

a data information processing circuit for receiving data information as an analog data signal including an analog sinusoidal signal and for processing said analog data signal, said data information processing circuit including,

A) an A/D converter for receiving said analog data signal from an input terminal and for converting said analog

data signal to a digital signal to output said digital signal from an output terminal;

B) a switch connected to said input terminal of said A/D converter; and

C) an offset cancel circuit, connected between said input terminal and output terminal of said A/D converter, for supplying a voltage to cancel an offset voltage of said A/D converter, said offset cancel circuit includes,

C1) a sampling control circuit for controlling said A/D converter in such a manner that first and third sampling intervals and second and fourth sampling intervals for said analog sinusoidal signal become 180 degrees when said analog sinusoidal signal is supplied to said A/D converter, whereby digital signals having first through fourth digital values are output from said A/D converter in a sampling order,

C2) an arithmetic operation unit for receiving one of a set of said first and third digital values and a set of said second and fourth digital values, and for computing an average value thereof to output said obtained average value as an offset voltage value for said A/D converter, and

C3) an offset voltage generator for receiving said offset voltage value, for generating an offset cancel voltage to cancel said offset voltage, and for supplying said offset cancel voltage to said A/D converter.

32. The signal processor according to Claim 31, wherein data information corresponding to said analog sinusoidal signal is a preamble pattern.

33. A method of canceling an offset voltage of an A/D converter for converting an analog signal to a digital signal, said method comprising the steps of:

detecting said offset voltage of said A/D converter based on a digital value of said digital signal; and

generating an offset cancel voltage for canceling said offset voltage.

34. A method of canceling an offset voltage of an A/D converter for converting an analog signal to a digital signal, said method comprising the steps of:

comparing a digital value of said digital signal with a predetermined offset allowance value, to determine an offset change amount;

accumulating said offset change amount when said digital value differs from said predetermined offset allowance value,

stopping said accumulating, to determine an accumulated offset change amount, when said digital value lies within said predetermined offset allowance value, and said offset change amount, and

generating an offset cancel voltage for canceling said offset voltage in accordance with said accumulated offset change amount.

35. A method of canceling an offset voltage of an A/D converter for sampling an analog data signal including an analog sinusoidal signal to convert said analog data signal to a digital signal, said method comprising the steps of:

using a control circuit for controlling said A/D converter in such a manner that first and third sampling intervals and second and fourth sampling intervals for said analog sinusoidal signal become 180 degrees when said analog sinusoidal signal is supplied to said A/D converter, whereby digital signals having first to fourth digital values are output from said A/D converter in a sampling order;

computing an average value of one of a set of said first and third digital values and a set of said second and fourth digital values, said obtained average value being an offset voltage value for said A/D converter; and

generating an offset cancel voltage to cancel said offset voltage in accordance with said offset voltage value.

36. A semiconductor integrated circuit device comprising:

an analog filter for removing an unnecessary frequency component included in an analog signal to produce a filtered analog signal; and

an A/D converter, connected to said analog filter, for performing over-sampling of said filtered analog signal according to a first frequency signal to convert said filtered analog signal to a digital signal.

37. The device according to Claim 36, further comprising:

a first digital filter, connected to said A/D converter, for removing an unnecessary frequency component included in said digital signal in accordance with said first frequency signal to produce a first filtered digital signal; and

a digital phase locked loop, connected to said A/D converter and said first digital filter, for generating said first frequency signal and for supplying said first frequency signal to said A/D converter and said first digital filter.

38. The device according to Claim 37, wherein said digital phase locked loop generates a second frequency signal lower than said first frequency signal, and said device further comprises a first register, connected to said first digital filter and said digital phase locked loop, for intermittently sampling said first filtered digital signal in accordance with

said second frequency signal to produce a first thinned digital signal.

39. The device according to Claim 38, wherein said digital phase locked loop includes:

a voltage controlled oscillator for generating said first frequency signal in response to a voltage signal; and

a frequency divider for frequency-dividing said first frequency signal to produce said second frequency signal.

40. The device according to Claim 39, further comprising a second digital filter, connected to said first sampling register and said digital phase locked loop, for removing an unnecessary frequency component included in said first thinned digital signal in accordance with said second frequency signal to produce a second filtered digital signal.

41. The device according to Claim 40, wherein said digital phase locked loop generates a third frequency signal lower than said second frequency signal, and said device further comprises a second register, connected to said second digital filter and said digital phase locked loop, for intermittently sampling said second filtered digital signal in accordance with said third frequency signal to produce a second thinned digital signal.

42. The device according to Claim 41, wherein said digital phase locked loop further includes:

a second frequency divider, connected to said first frequency divider, for frequency-dividing said second frequency signal to produce said third frequency signal.

43. The device according to Claim 37, wherein said digital phase locked loop includes:

a phase difference detector for comparing a value of said first thinned digital signal from said first register with a reference value to detect a phase difference between an actual sampling point for said first filtered digital signal and an optimal sampling point; and

an adjusting unit, connected to said phase difference detector, for adjusting said second frequency signal based on said phase difference in such a way that said actual sampling point substantially matches with said optimal sampling point.

44. The device according to Claim 43, wherein said adjusting unit adjusts said second frequency signal by performing one of insertion of a pulse into said first frequency signal and deletion of a pulse from said first frequency signal.

45. The device according to Claim 43, wherein said phase difference detector includes:

an inclination computing circuit for computing an inclination of a wave form of said first thinned digital signal at said actual sampling point;

a comparator for comparing a first reference value with a value of said first thinned digital signal;

an estimation circuit, connected to said inclination computing circuit and said comparator, for estimating one among a plurality of optimal sampling points closest to said actual sampling point, based on said computed inclination, a comparison result and a sign associated with said first thinned digital signal; and

a phase determining circuit, connected to said estimation circuit, for detecting a phase difference between said actual

sampling point and said estimated optimal sampling point based on said estimated optimal sampling point, a value of said first thinned digital signal and a reference value.

46. The device according to Claim 42, wherein said digital phase locked loop includes:

a phase difference detector for comparing a value of said first thinned digital signal from said first register with a reference value to detect a phase difference between an actual sampling point for said first filtered digital signal and an optimal sampling point; and

an adjusting unit, connected to said phase difference detector and said first frequency divider, for adjusting said second frequency signal based on said phase difference in such a way that said actual sampling point substantially matches with said optimal sampling point, wherein said adjusting unit adjusts said second frequency signal by performing one of insertion of a pulse into said first frequency signal and deletion of a pulse from said first frequency signal.

47. The device according to Claim 46, further comprising a control circuit, connected to said phase difference detector and said voltage controlled oscillator, for performing frequency control of said first frequency signal in accordance with said detected phase difference after said actual sampling point substantially matches with said optimal sampling point.

48. A method of performing a digital signal process comprising the steps of:

sampling an analog signal according to a first frequency signal,

converting said analog signal to a digital signal, and

performing a digital signal process on said digital signal according to a second frequency signal lower than said first frequency signal.

49. The method according to Claim 48, further comprising the step of:

removing an unnecessary frequency component included in said analog signal.

50. The method according to Claim 49, wherein said digital signal process includes,

intermittently sampling said digital signal in accordance with said second frequency signal to produce a thinned digital signal.

add B3

add C4